Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 8-16 and 30 are allowed.

Anticipation Rejection

The Examiner has rejected claim 24 under 35 U.S.C. § 102(b) as being anticipated by JP 11-307724 (hereinafter "JP '724"). This rejection is respectfully traversed.

JP '724 discloses a semiconductor integrated circuit wherein an input protective circuit is arranged below bonding pads to reduce the chip size. (*See* English Language Abstract). More specifically, FIGS. 1-3 show an input section 12 wherein three wiring layers 36, 38 and 40 are buried in insulating layers 30a-c and 42. These wiring layers 36, 38 and 40 form an input protection circuit 12a. (*See* par. [0013]).

The Examiner takes the position that JP '724 discloses all of the features of claim 24.

In contrast, Applicants respectfully submit that JP '724 fails to teach or suggest *at least* "a pad area (13) surrounding the inner area (11)" of the semiconductor device, as recited in claim 24. Specifically, JP '724 only vaguely discloses an inner portion, and completely fails to teach or suggest any specifics of this portion. Further, JP '724 fails to disclose a pad area "surrounding" this undescribed inner area. JP '724 only discloses that an input section 12 is arranged at the circumference (see par. [0010]). A portion simply disclosed as being arranged at the circumference cannot teach or suggest "surrounding" an inner area.

Thus, Applicant respectfully submits that independent claim 24 is patentable over the applied reference, and respectfully requests that the Examiner withdraw this rejection.

Obviousness Rejection

The Examiner has rejected claims 3, 25 and 26 under 35 U.S.C. § 103(a) as being unpatentable over JP '724 in view of JP 05-55380 (hereinafter "JP '380"). This rejection is respectfully traversed.

JP '724 is discussed in detail above. JP '380 discloses a semiconductor integrated circuit device with a power supply wiring layer 9 formed on an upper surface thereof. The power supply wiring layer 9 is formed inside of a pad area, and is arranged above a laminated structure 8 so that the power supply wiring layer 9 functions as a bypass capacitor.

The Examiner takes the position that JP '724 discloses many of the features recited in claims 3, 25 and 26, but fails to teach or suggest "that the wiring layers are connected as a bypass capacitor." Applicant agrees that JP '724 fails to teach or suggest such features.

Nevertheless, the Examiner applies JP '380, taking the position that it discloses "that connection of wiring layer 9 to the power supply voltage and connection of wiring layer to ground will create a bypass capacitor using the two stacked wiring layers." (*See* Office Action, pg. 3, numbered paragraph 3). Additionally, the Examiner alleges that one of skill would have been motivated to modify JP '724 with JP '380 because "such a configuration will suppress power source noise."

As an initial matter, Applicant respectfully submits that there would have been no motivation to modify JP '724 with the system of JP '380. Specifically, there is no teaching or suggestion that JP '724 includes such a power supply wiring layer 9 that could utilize the laminated structure 8. Accordingly, one of skill would not have looked to JP '380 to modify JP '724.

Additionally, even if JP '724 could have been modified in view of JP '380, Applicant respectfully submits that even the resultant combination would fail to teach or suggest all of the features recited in claims 3, 25 and 26.

Specifically, Applicant respectfully submits that the resultant combination fails to teach or suggest at least that "a second device [is] fabricated below the device," (where the device is a bypass capacitor and the second device is, for example, a protection device or an input/output device) as recited in claim 3, 25 and 26. Specifically, even if the bypass capacitor of JP '380 and the protection circuit of JP '724 could have been provided in the same chip, there is no teaching or suggestion that one would be provided above or below the other. In contrast, it seems clear that the bypass capacitor would have been provided beneath a wiring line, and the protection circuit would have been provided under a pad. Thus, the bypass capacitor and the protection circuit would have been provided laterally adjacent to each other, and not above or below one another.

Thus, Applicant respectfully submits that independent claims 3, 25 and 26 are patentable over the applied references, and respectfully requests that the Examiner withdraw this rejection.

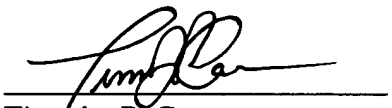
Conclusion

In view of the foregoing, it is respectfully submitted that claims 3, 8-16, 24-26 and 30 are allowable. Thus, it is respectfully submitted that the application now is in condition for allowance with all of the claims 3, 8-16, 24-26 and 30.

If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees which may be required to maintain the pendency of this application, except for the Issue Fee, to our Deposit Account No. 19-4880.

Respectfully submitted,



Timothy P. Cremen
Registration No. 50,855

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: November 6, 2003